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Teseda and Mentor Graphics Partner to Speed Defect Diagnosis

PORTLAND, Oregon _ October 24, 2008 _ Teseda Corporation, a leading silicon validation and failure analysis diagnostic company, announced today that they have partnered with Mentor Graphics to link Mentor Graphic's YieldAssist toolset with the Teseda Diagnostic Environment. This new capability will provide Teseda and Mentor customers with an integrated and truly layout-aware roundtrip flow that will accelerate their ability to rapidly diagnose scan failures down to the yield-limiting defects, and identify those defects in the physical layout. The portability and low cost of the Teseda platform will allow more users access to the new iterative diagnosis capability in YieldAssist. Coupled with the massive failure capture memory in the Teseda V-series systems, the YieldAssist tool will be able to iterate on even the most data-intensive defect candidates, such as defects in the scan logic.

The Teseda TWB Software will process test patterns from Mentor Graphics ATPG tools and run them directly on any Teseda TWB supported platforms, including the V520 and V550. The failure files are then passed to YieldAssist to analyze the test response and identify defect candidates. The resulting defect candidates can then be shown in the Teseda NetXY physical viewing environment. Optionally, the YieldAssist tool may be instructed to further isolate the candidates down to the most probable defect(s) by producing an iterative pattern set which can be immediately applied to the device-under-test through the Teseda Platform. This iterative process will yield the most probable defect candidate(s), which again may be highlighted in Teseda's NetXY physical viewing environment.

"We are pleased to work with Mentor Graphics to link the YieldAssist toolset to the Teseda Diagnostic Environment," said Armagan Akar, CEO of Teseda. "This partnership allows us to work together to accelerate diagnosis of yield-limiting defects for our mutual customers."

"The integration of YieldAssist's true layout-aware diagnosis capability and iterative diagnosis flow with Teseda's Diagnostic Environment provides added value to our mutual customers," said Greg Aldrich, Director of Marketing of the Design-For-Test Division of Mentor Graphics. "The seamless flow of information between tools allows users to study the actual defect polygons computed by YieldAssist in Teseda's NetXY physical viewing environment, significantly reducing the time required for a positive identification of physical defects and yield limiters."

Both Teseda and Mentor Graphics will be demonstrating the new capability at the upcoming International Test Conference (ITC) in Santa Clara, CA and the International Symposium on Test and Failure Analysis (ISTFA) in Portland, OR.

About Teseda Corporation

Teseda's products allow its customers to speed silicon debug, manufacturing ramp, failure analysis, and yield learning. The validation and diagnostic solutions allow Teseda's customers to achieve Rapid Silicon Validation (Time to Market), Rapid Defect Analysis (Time to Volume) and Yield Assurance (Continued Volume). Teseda is headquartered in Portland, Oregon. For more information about Teseda, its products and distribution network, please call 503.223.3315 or visit www.teseda.com